APPLICATION NOTE

A 75W Quasi Resonant TEA1506 based flyback Converter for TV Applications

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Abstract

The present application note describes a typical TV / Monitor power supply, based on a GreenchipII™ controller, the TEA1506. The features of this controller are elaborated in full detail and a possible design strategy is given to obtain the basic component values..

APPLICATION NOTE

A 75W Quasi Resonant TEA1506 based flyback Converter for TV Applications

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1. INTRODUCTION

1.1 A TYPICAL TV / MONITOR POWER SUPPLY

This application note will focus on a Switched Mode Power Supply (SMPS) intended for a general 75W TV/Monitor. Characteristic for this type of power supply is the combination of both high and low voltage outputs. A more detailed specification is given in APPENDIX 1. Although not detailed in this application note, the GreenChipII controller family can be used for various types of Flyback, Forward and Buck converters depending on the creativity of the Switched Mode Power Supply designer.

Different topologies (resonant LLC, hard-switching flyback, Quasi Resonant flyback etc.) can be used to realize an SMPS as described above. The combination of universal mains, low cost and high efficiency implies more or less for a Quasi Resonant flyback converter

- A wide input voltage range can be covered since both duty-cycle and switching frequency are varied to control the output power.
- Low cost by a low component count (only one secondary diode and one primary MOSFet).
- High efficiency because of the resonant behaviour (soft/semi-soft switching-on of the primary MOSFet).

The GreenChipII flyback controller can perfectly be used to address those specification items and covers also all the necessary protections without extra external components.

1.2 THE GREENCHIP^{TM}II FAMILY

The GreenChip^{TM}II (TEA1506, TEA1507, TEA1533, TEA1552) is a variable frequency SMPS controller designed for a Quasi-Resonant Flyback converter operating directly from the rectified universal mains. The topology is suitable for TV and Monitor Supplies in particular, but can be used for high efficient Consumer Electronics SMPS as well. The power supply operates in a critical conduction mode (border continuous/discontinuous mode of operation) at nominal output loads including zero/low voltage switching (ZVS/LVS). The ZVS/LVS is achieved by the resonant behaviour of the voltage across the power switch and is therefore often referred to as Quasi-Resonant mode of operation. A novel valley detection circuitry implemented in the controller results in exact valley switching under all conditions.

The control method used in the GreenChip^{TM}II is of the Current Mode Control type, which has the benefit of inherent line frequency ripple rejection. Control takes place by comparing the sensed primary current with the error voltage that is present on the Ctrl pin (V_{CTRL}) to generate the primary “on” time. At higher and nominal output powers the switching frequency is depended on the input voltage and the output load. The MOSFet is switched on only if the transformer core is completely demagnetized and the drain voltage is at it’s minimum (valley detection) which results in zero- or low voltage switching to enhance the supplies’ efficiency . The GreenChip^{TM}II is intended to be used in combination with secondary control (opto-coupler feedback) resulting in a very accurate control of the output voltage at all load conditions and load transients.

Standard two different types of stand-by modes are provided. The first is Reduced Frequency Mode of Operation, which is detected by means of the control voltage and minimizes the switching losses at

low output loads. This feature enables the possibility for no load power consumption levels below 3W for this type of power supplies and no additional circuitry is needed. A second standby mode for extreme low power consumption at no load is called cycle skipping mode of operation.

The key features of the TEA1506 are summarized below in no special order

Distinctive features

- Operates from universal mains input $85V_{AC} - 276V_{AC}$
- High level of integration leads to a very low external component count
- Soft (re)Start to prevent audible noise (externally adjustable)
- Leading Edge Blanking (LEB) for current sense noise immunity

Green features

- Extreme low quiescent current during start-up (<50μA), enabling high ohmic start-up resistors
- Valley (zero/low voltage) switching for minimal switching losses
- Frequency Reduction at low output powers for improved system efficiency (power consumption < 3W, P_o=5V@20mA)
- Cycle Skipping Mode of operation for extreme low, no load power levels

Protection features

- Safe-Restart mode for system fault conditions
- Under Voltage Protection (UVLO) for foldback during overload
- Continuous mode protection by means of demagnetization detection
- Accurate Over Voltage Protection (OVP) (external adjustable)
- Cycle-by cycle Over Current Protection (OCP)
- Input voltage independent Over Power Protection (OPP)
- Short Winding Protection (SWP)
- Maximum T_{on} Protection
- Over Temperature Protection (OTP)
- Open and short IC pin protections

These features enable the power supply engineer to design a reliable and cost effective SMPS with a minimum number of external components and the possibility to deal with the high efficiency requirements.

2. FUNCTIONAL DESCRIPTION OF THE TEA1506

2.1 TEA1506 VERSUS TEA1507

Below a change list is given in order to enable a quick usage of the TEA1506 by experienced TEA1507 users.

- **Added Cycle Skipping Mode function**

Cycle skipping mode will be activated at very low power levels.

- **Changed Fmin**

Fmin has been increased from 6.5kHz to 25kHz.

- **Demag pin open / not connected protection**

When the demag pin is open / not connected an undefined situation can occur. Since the IC is not receiving demag information, the power mosfet can be switched on while the transformer is not demagnetised yet. That can overheat the mosfet due to severe turn-on loss.
The solution for this problem is made internally by a very small bleeder current to the pin, which ensures that the pin voltage is always above the demag detection level when left open. This results in a “continuous demag" situation for the IC, which prevents switching.

- **Vctrl pin open / not connected protection**

When the Vctrl pin is open / not connected an undefined situation can occur. Since the IC is not receiving feedback information from the output, the power supply can operate at any level of power, independent of the output voltage or output load.
The solution for this problem is applying a bleeder current to the pin, which ensures that the pin voltage is always high and as a result a minimal duty cycle or cycle skipping is activated. The supply will operate in the safe restart mode.

- **Removed High Voltage start-up current source**

The high voltage start-up current source is removed for cost reasons. Still a high voltage pin is present for “true” valley detection.

- **Removed burst mode**

The burst mode has been removed for cost down reasons. Still a low standby power can be achieved by using the cycle skipping feature. Input power below 2W can be feasible.

- **Mains detection level (Mlevel) function has been removed**

This function has also been removed for cost down reasons.

- **The driver sink- and source capability have been decreased by roughly 20%**

The driver capability has been decreased for cost down reasons, but is considered still to be powerful enough to drive large power Fets commonly used in TV / Monitor applications (e.g. STP7NB80)

2.2 START-UP SEQUENCE

2.2.1 Charging Vcc capacitor

The major difference between the TEA1507 and the TEA1506 is the start-up sequence due to the absence of a High Voltage currents source and the Mains Enabling level. The initial start-up current, which charges the Vcc capacitor to Vcc start-up level, will be drawn from the mains as depicted in the example below.

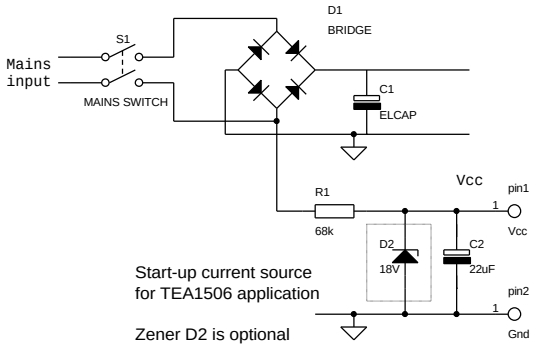


Fig. 2-1 The most "basic" start-up circuit.

Start-up time inversely proportional with mains voltage.

The V_{cc} capacitor is charged from half the mains voltage, i.e.

$$V_{charge} = \frac{\sqrt{2}}{p} V_{AC} \qquad (2.1)$$

in which V_{AC} is the mains voltage level.

The Vcc current -Icc- drawn by the IC is > 0.8mA when it has started-up. If the external charge current exceeds the Icc current than Vcc keeps ramping up which must be limited by an external <20V zenerdiode to obey the Vcc maximum voltage rating of 20V. Also this condition has a consequence for the protection modes. When triggered the IC does not enter the safe restart cycle. For a restart the Vcc uvlo level has to be reached but Vcc is not discharged. It means that the protection mode is latched. Then a supply restart is only possible by switching the mains off and on again.

If a latching protection mode is not wanted than a minimum value for R1 has to be determined. The supply start-up delay is directly linked herewith.

Conditions for the minimum value of the charge resistor R1 are;
Maximum specified mains voltage, Vac_max., and the limit in charge current, Icharge_max.

The resistor R1 is calculated by;

$$R_{1\_\min} = \frac{\frac{\sqrt{2}}{p} V_{AC}^{\max} - V_{uvlo}}{I_{charge\_\max}} \quad (2.2)$$

in which;
Vuvlo = 8.7V ,the Vcc under voltage level. For Icharge_max take ≤0.8mA.
Vac_max depends on the mains input range and common values are;

Table.1

Nominal mains	Mains range
Single 115Vac	138Vac_max to 90Vac_min
Single 230Vac	276Vac_max to 150Vac_min
Wide mains	276Vac_max to 90Vac_min

Based on the calculated value for R1 a practical -not lower- value can be chosen.
Then the longest delay in supply start-up can be calculated by;

$$t_{delay\_\max} = -R_1 C_2 \ln\left(1 - \frac{V_{cc\_start}}{\frac{\sqrt{2}}{p} V_{AC}^{\min}}\right) \quad (2.3)$$

in which C_2 is the Vcc capacitor (usually 22µF) and Vcc_start the start up voltage level (11V). For Vac_min common values see the listing above.

The maximum loss in resistor R1 occurs at the high mains, Vac_max;

$$P_{loss(R1)} = \frac{\left(\frac{\sqrt{2} \cdot V_{AC}^{\max} - V_{cc}}{2}\right)^2}{R_1} \quad (2.4)$$

Vcc is the operational voltage from the take-over supply, ~14V as example.

For the most common mains input specifications a listing is given of the results by the formulae given above.

Table 2

C_{Vcc}=22uF	Single mains		Single mains		Wide mains	
	115Vac		230Vac		90 - 276Vac	
	90Vac	138Vac	150 Vac	276Vac	90Vac	276Vac
R1_min	72k		144k		144k	
R1 practical	**75k**		**150k**		**150k**	
t delay	**0.57s**	**0.34s**	**0.61s**	**0.31s**	**1.14s**	**0.31s**
Icharge	0.49mA	077mA	0.39mA	0.77mA	0.21mA	0.77mA
R1_loss	42mW	105mW	64mW	232mW	21mW	232mW

For a different Vcc capacitor value the start up delay time scales in proportion with $\frac{C_{applied}}{22uF}$.
By increasing the value of R1 than proportionally the delay time increases and the R1_loss decreases.

For fail safe purpose, an optional 18V zenerdiode can be added to limit the maximum Vcc voltage.

2.2.2 Charging soft start capacitor

The soft start switch (fig. 2.1) is closed at the moment the V_{CC} capacitor voltage level reaches 7V (typ.). This level initiates the charging of the soft start capacitor, V_{SS}, up to a voltage level of 500mV with a typical current of $60mA$. In the mean time the V_{CC} capacitor is continued to be charged in order to reach the V_{CC} start-up level. Once the V_{CC} capacitor is charged to the start-up voltage level (11V typ.) the TEA1506 controller starts driving the external MOSFet and the soft start current source is switched off. Resistor R_{SS} will discharge the soft start capacitor, C_{SS}, resulting in an increasing amplitude of the primary peak current to its steady state value in normal mode of operation. This smooth transition in current level will limit audible noise caused by magnetostriction of the transformer core material. The time constant of the decreasing voltage across C_{SS}, which is representing the increasing primary peak current, can be controlled with the RC combination R_{SS}/C_{SS}.
To use the total soft start window, R_{SS} should be chosen

$$R_{SS} > \frac{V_{OCP}}{I_{SS}} = \frac{500mVtyp}{60\mu Atyp} = 8.7k\Omega,$$

(2.5)

and from

$$i_s = C_{V_{CC}} \frac{dV_{CC}}{dt_s} \rightarrow dt_s = \frac{C_{V_{CC}} \left(V_{CC\_start} - V_{CC\_softstart}\right)}{i_s},$$

$$i_{ss} = C_{SS} \frac{dV_{C_{SS}}}{dt_{ss}} \rightarrow dt_{ss} = \frac{C_{V_{C_{SS}}} V_{C_{SS}}^{max}}{i_{ss}},$$

$$dt_{ss} < dt_s \rightarrow C_{SS} < 0.4C_S.$$

(2.6)

a appropriate soft start capacitor can be chosen, in order to be sure that C_{SS} is pre-charged to it's maximum level of 500mV. During start-up phase the V_{CC} capacitor will be used to deliver the necessary energy to power the TEA1506 up till the moment the auxiliary winding overtakes.

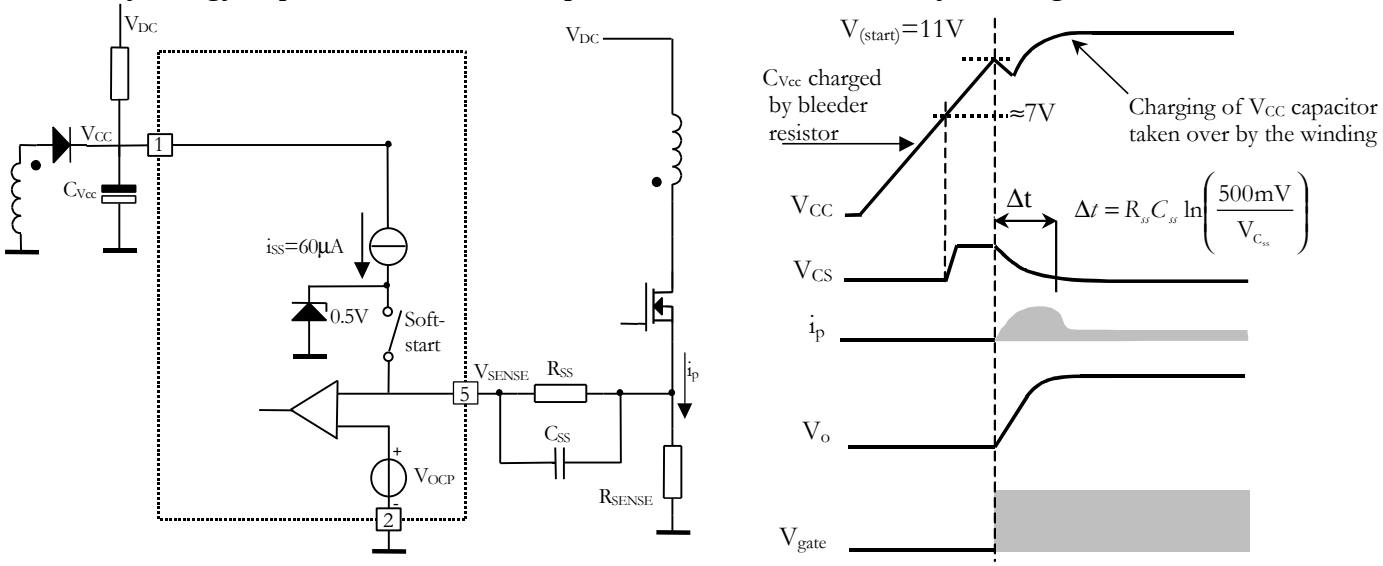


Fig. (2.1) Start-up charging of C_{Vcc} and soft start control.

2.3 MULTI MODE OPERATION

In order to achieve the highest efficiency possible at various output loads, the TEA1506 is able to operate in five different modes, which are listed below in order from maximum output power to no load.

1. Quasi-Resonant (QR-mode) mode of operation
2. Fixed Frequency (FF-mode) mode of operation
3. Frequency Reduction (VCO-mode) mode of operation
4. Minimum Frequency (MF-mode) mode of operation
5. Cycle skipping / Automatic Burst (AB-mode) mode of operation

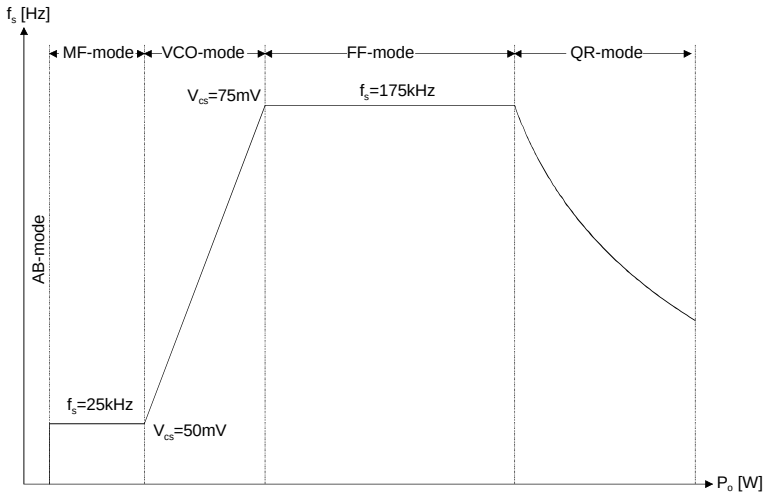


Fig. (2.2) The switching frequency versus output power. Each power level corresponds with a different mode of operation.

QR-mode is the most appropriate mode of operation at high output loads. Switching on of the MOSFet is only allowed at the minimum of the drain-source voltage (LVS/ZVS) which reduces the switching losses ($P_{sw} = \frac{1}{2} C_{ds} V_{ds}^{\ 2} f_s$) resulting in an improved efficiency performance. EMI will be improved for two reasons when operating in QR-mode. First the current spike due to discharging of the resonant capacitor, C_{ds} , is lower, since the voltage at switching on is lower due to LVS/ZVS. Secondly the switching frequency is modulated with the double mains frequency and can be approximated by

$$f_s = \frac{h}{2 P_o L_p} \left(\frac{N V_{DC} \left(V_o + V_F \right)}{N V_{DC} + V_o + V_F} \right).$$

(2.7)

This effect causes the EMI spectrum to be spread over the frequency band, rather than being concentrated on a single frequency value.

FF-mode is an improvement on the normal behavior of a QR-mode power supply that tends to increase the switching frequency to very high levels at the moment the output power is reduced. In FF-mode the switching frequency is fixed to a predefined level avoiding this unwanted frequency increase. Valley switching is still active in this mode of operation, increasing the overall efficiency of the power supply.

FR-mode is implemented to decrease the switching losses at low output loads. In this way the efficiency at low output powers is increased, which enables lower power consumption The voltage at the Ctrl pin determines the onset of frequency reduction. An external Ctrl voltage of 1.425 V corresponds with an current sense level of 75mV. The frequency will be reduced linear with the current sense level (At current sense levels higher than 75mV, Ctrl voltage < 1.425V, the oscillator will run on maximum frequency f_{oscH} = 175kHz typically). At a current sense level of 50mV, V_{CTRL} = 1.450V, the frequency is reduced to the minimum level of 25kHz. Valley switching is still active in this mode.

MF-mode

At current sense levels below 50mV (V_{CTRL}>1.450V), the minimum frequency will remain at 25 kHz.

AB-mode
At current sense levels below 41mV (V_{CTR}>1.459V), switch on of the external MOSFet is inhibited and as a result switching cycles are left out. As soon as the control voltage has dropped below 1.459V, the power supply starts switching again. The time constant of the feedback loop will determine the number of switching cycles.

2.4 SAFE-RESTART MODE

This mode is introduced to prevent destruction of components due to excessive heat generation during system faults (fault condition tests) and is used for Burst mode of operation as well. The Safe-Restart mode will be invoked after being triggered by the activation of one of the next functions

1. Over Voltage Protection
2. Short Winding Protection
3. Maximum “on time” Protection
4. V_{CC} reaching UVLO level
5. Over Temperature Protection

When entering the Safe-Restart mode the output driver is immediately disabled and latched, that means the SMPS stops switching and is locked in this state. The auxiliary winding will not keep the V_{CC} capacitor charged anymore and the V_{CC} voltage will drop until UVLO is reached. Then the V_{CC} capacitor will be recharged via the start-up circuitry and a new start-up sequence as described in paragraph 2.2 will be initiated. The TEA1506 will remain in this Safe Restart mode until the fault condition is removed.

2.5 PROTECTIONS

2.5.1 Demagnetization sense

This feature guarantees discontinuous conduction mode operation at any time in any mode of operation. This function prevents the transformer core to saturate and continuous mode of operation during initial start-up and when overloading the output. The demag(netization) sense is realized by an internal circuit that guards the voltage (V_{demag}) at pin 4 that is connected to auxiliary winding by resistor R_1. Fig. (2.3)shows the circuit and the idealized waveforms across this winding.

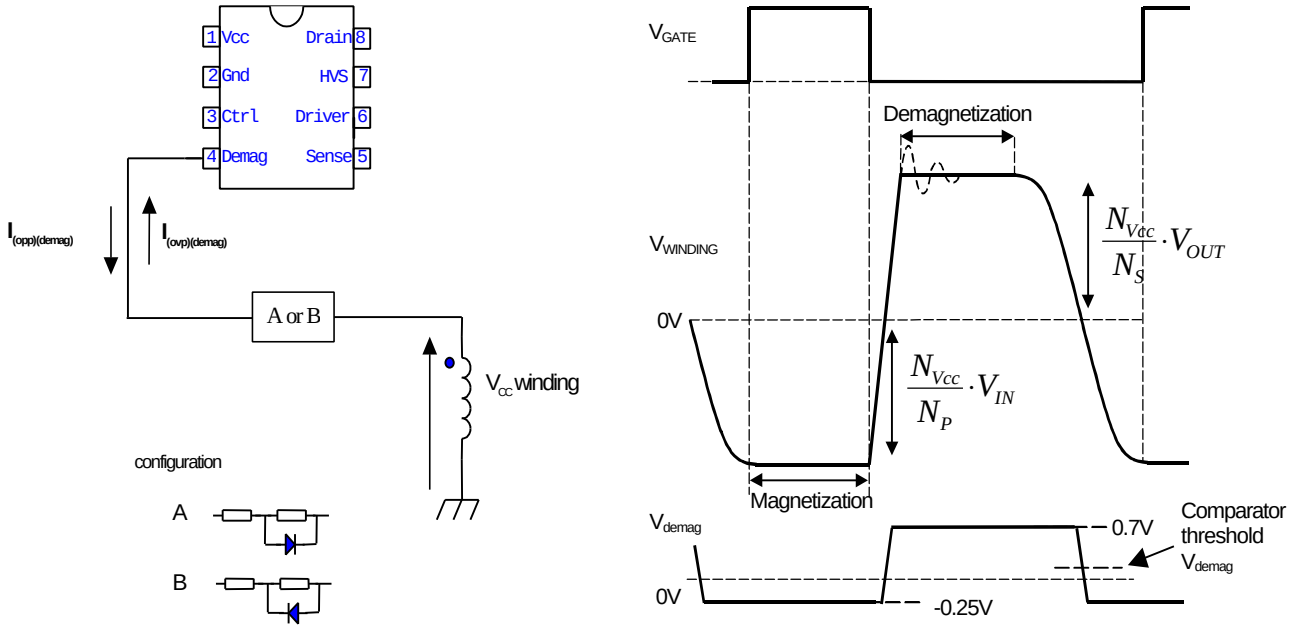


Fig. (2.3) Demagnetisation sensing and relevant waveforms.

Configuration A is used if the required OPP resistor value is lower than the required OVP resistor value.

Configuration B is vice versa.

As long as the secondary diode is conducting (demagnetization of transformer), the auxiliary winding voltage is positive (flyback stroke). In this case V_{demag} is also positive and clamped at a level of 700mV. The controller will force the driver output to remain in “off” mode as long as the voltage at pin 4 is positive and above 100mV. This means that the switching frequency has the possibility to decrease in case of start-up or overload condition. After demagnetization the reflected output voltage at the auxiliary winding starts oscillating since it is well coupled with the primary winding and therefore reflecting the $L_p C_{ds}$-oscillation, which occurs after the flyback stroke. When the voltage condition $V_{demag} < 100mV$ is met the controller will wait for valley detection to allow the start of a new switching cycle.

In order to limit the total number of pins, novel OVP and OPP functions are implemented using the same IC pin. These two protections determine the resistor values of R_1 and R_2.

NOTE: There are two configurations to be considered. Dependent on the highest resistor value (R_1 or R_2) one should choose the direction if the diode. See configuration A and B in Fig. (2.3).

2.5.2 Over Voltage Protection

The Over Voltage Protection ensures that the output voltage will remain below an external adjustable level. This is realized by sensing the reflected output voltage across the auxiliary winding by means of the current flowing into the demagnetization pin. This reflected voltage is related to the output voltage

via to the turns ratio of the auxiliary winding (n_a) and the secondary winding (n_s). The maximum output voltage is set by the resistor value R_1 that determines the positive current flowing into the demagnetization pin of the TEA1506. This current is compared with an internal threshold level of $60mA$ (typ.) and exceeding this level will trigger the OVP function. R_1 can be calculated with

$$R_1 = \frac{\frac{n_a}{n_s}\left(V_{o\_OVP} + V_F\right) - V_{dem\_clamp\_pos}}{i_{dem\_OVP}},$$

(2.8)

in which n_a is the number of auxiliary turns, n_s is the number of secondary, V_{o_OVP} is the OVP output voltage level, $V_{dem\_clamp\_pos}$ is the positive clamp voltage of demagnetization input (700mV typ.), V_F is the forward voltage drop of the auxiliary diode and i_{dem_OVP} is the current threshold of the OVP protection (60µA typ.)

After triggering the OVP function, the driver is disabled and the controller enters a Safe-Restart mode. The controller will remain in this state as long as an over-voltage condition is present at the output. The dashed line in Fig. (2.3)shows a more practical waveform of the auxiliary winding. The ringing is caused by the $L_s C_{ds}$ oscillation. To compensate this ringing (load dependent) the current into the demagnetization pin is integrated over the flyback time interval. This method increases the accuracy of the OVP detection level and prevents false triggering.

2.5.3 Over Current and Over Power Protection

The maximum output power limitation needs some special attention when using a Quasi-Resonant converter. The maximum output power is not only function of the primary peak current $\hat{i}_p$, but of the input voltage, V_{DC} as well. Eq.(2.9) shows the relation between input voltage and output power (the resonance time is neglected).

$$P_{O\_MAX} = \eta \cdot \frac{\hat{i}_p}{2} \cdot \left(\frac{N\left(V_o + V_F\right)V_{DC}}{N\left(V_o + V_F\right) + V_{DC}} \right),$$

(2.9)

The maximum output power will increase with the input voltage when the OCP level would be a fixed level. To prevent over dimensioning of all the secondary power components an internal OCP compensation is used to get an independent OPP level. This compensation is realized by sensing the input voltage level via the auxiliary winding, since $V_a = \left(n_a / n_p\right)V_{DC}$ during the primary “on” time. A resistor is connected between this winding and the demagnetization pin. During magnetization of the transformer the reflected input voltage is present at this winding (see Fig. (2.3)). A negative current into this pin is used to compensate the OCP level. Fig. (2.4)shows the relation between the negative current and OCP level.

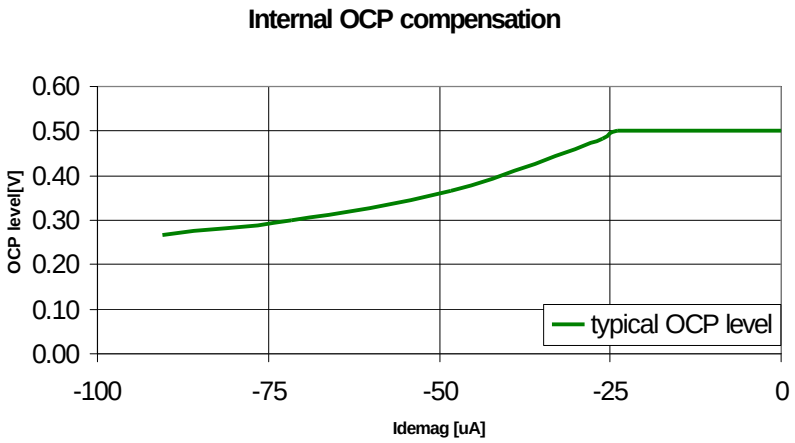


Fig. (2.4) Internal OCP compensation

The current threshold level where the controller starts to compensate the OCP level is fixed at - 24µA. This threshold level is used to set the external resistor value at the minimum input voltage, leading to

$$R_2 = \frac{V_{DC\_\min}\frac{n_a}{n_p} - V_{dem\_clamp\_neg}}{i_{dem\_OPP}}, \qquad (2.10)$$

in which n_a is the number of auxiliary turns, n_p is the number of primary turns, $V_{DC\_\min}$ is the minimum DC input voltage, $V_{dem\_clamp\_neg}$ is the negative clamp voltage of demagnetization pin (-250mV typ.) and i_{dem_OPP} is the internal current threshold of OPP correction (-24µA typ.)

2.5.4 Short Winding Protection

The short winding protection is implemented as a protection for shorted transformer windings, for example in case of a secondary diode short. In this case the primary inductance is shorted out and the primary current starts to rise at very high rate (only limited by the leakage inductance) after switch-on of the MOSFET. An additional comparator (fixed threshold of $V_{swp} = 880\text{mV}$) implemented in the IC will detect this fault condition by sensing the voltage level (via pin 5) across the sense resistor. Immediately the driver is disabled and the controller enters the Safe-Restart mode. This protection circuit is activated after the leading edge blanking time (LEB).

2.5.5 LEB and maximum “on-time”

The LEB (Leading Edge Blanking) time is an internally fixed delay preventing false triggering of the comparator due to current spikes that are present at the current sense voltage. This delay determines the minimum “on time” of the controller. This minimum on time together with the minimum switching frequency and the primary inductance defines the minimum input power at which the output voltage is

still in regulation. Because this minimum frequency is low it is possible to run at extremely low loads (without any pre-load).
The IC will protect the system against an “on-time” longer then 50µs (internally fixed maximum “on-time”). When the system requires on times longer than 50µs, a fault condition is assumed, and the controller enters the Save-Restart mode.

2.5.6 Over Temperature protection

When the junction temperature exceeds the thermal shutdown temperature (typ 140°C), the IC will disable the driver and will or enter Safe Restart mode or is latched. When the V_{CC} voltage drops to UVLO, the V_{CC} capacitor will be recharged to the V_{start} level. If the temperature is still too high, the V_{CC} voltage will drop again to the UVLO level (Safe-Restart mode). This mode will persist until the junction temperature drops 8 degrees typically below the shutdown temperature.

2.6 PIN DESCRIPTION

SYMBOL	PIN	DESCRIPTION
Vcc	1	This pin is connected to the supply voltage. An external start-up circuit charges the V_{CC} capacitor and normal operation is initiated when the voltage reaches a level of 11V. The output driver is disabled when the voltage gets below 9V(UVLO). Operating range is between 9V and 20V.
Gnd	2	This pin is ground of the IC.
Ctrl	3	This pin is connected to the feedback loop. The pin contains two functions, i.e. primary current control and standby mode selection. Between 1V and 1.425V it controls the on time. The frequency is reduced starting from a level of 1.425V up till 1.450V, where the frequency is equal to the minimum frequency of the oscillator (25kHz). From a level of 1.459V and up switching cycles are left out and Automatic Burst mode of operation starts.
Demag	4	This pin is connected to the V_{CC} winding. The pin contains three functions. During magnetization the input voltage is sensed to compensate the OCP level for OPP (independent of input voltage). During demagnetization the output voltage is sensed for OVP and a comparator is used to prevent continuos conduction mode when the output is overloaded.
Sense	5	This pin contains three different functions. Soft start, protection levels OCP (OPP) and SWP. By connecting an R_{SS} and C_{SS} between the sense resistor and this pin it is possible create a Soft start. Two different protection levels of 0.5V(this OCP level depends on the Demag current) and 0.88V(fixed SWP level) are implemented.
Driver	6	This pin will drive the switch (MOSFET). The driver is capable of sourcing and sinking a current of respectively 135mA and 560mA.
HVS	7	This is a High Voltage Spacer (keep this pin floating)
Drain	8	This pin is connected to the drain of the switch or center-tap of the transformer depending on the voltage (BV_{DSS} = 650V). The main function of this pin is valley detection for zero/low voltage switching.

Table 2.3 Pin description

3. DESIGN OF A 75 WATT QUASI RESONANT POWER SUPPLY

3.1 DIMENSIONING THE KEY COMPONENTS

This chapter can be used as a guide to calculate the large signal components of the Quasi-Resonant converter including the primary transformer inductance L_P the resonance capacitor C_D and the current sense resistor.
This design strategy is used to design a monitor supply (see circuit diagram, page). It will be clear that the strategy differs in each application depending on costs, volume, efficiency etc.

Calculating the transformer inductance L_P and the resonance capacitor C_D two important requirements are used:
Universal input range $85V_{AC}$…$264V_{AC}$;
Operating power range 20W…$85W_{peak}$.

Due to efficiency reasons the converter has to operate in the Quasi-Resonant mode within this power range, which makes it possible to achieve efficiency up to 90%.

There are also some other choices and criteria that have to be taken care of before starting the design. These choices strongly depend on the application as mentioned before.

- No peak clamp to limit the maximum voltage across the switch. Minimize component count and improve efficiency;
- maximum voltage across the power MOSFET (V_{D_MAX}, including ΔV caused by leakage inductance L_s) which defines maximum turns ratio n;
- f_{MIN} = 25kHz and f_{MAX} = 150kHz. The choice of f_{MIN} determines the transformer size and f_{MAX} is restricted by the maximum frequency of the controller.

Some additional requirements should be taken into account:

- dV/dt drain source < 4kV/us (EMI reduction)
- Maximum permitted on-time < 50us ($t\text{-}on_{max}$ = 50us fixed by IC)

Eventually there are five different parameters to design:

- Turns ratio n;
- Primary inductance L_P and resonance capacitor C_D;
- Volt/turn to get the required voltages at the output;
- Core size (A_{eff} effective core surface).

In the following description the parameters are defined step by step.

Step 1 Maximum turns ratio n

The turns ratio should be as large as possible to get zero voltage switching also at high input voltages. This will reduce the switching losses of the MOSFET. However the turns ratio is restricted by the choice of the breakdown voltage of the MOSFET. In this case an 800V MOSFET is chosen because of the wide input voltage range (85Vac – 264Vac) and an additional spike caused by the leakage

inductance of the transformer (no peak clamp is used). This means that the maximum drain voltage should be lower than 800V including the voltage caused by the leakage inductance L_S. The maximum drain source voltage is equal to

$$V_{D\_MAX} = V_{IN\_MAX} + n \cdot (V_{OUT} + V_F) + \Delta V \ . \quad (3.1)$$

in which ΔV (caused by the leakage inductance) can be estimated by

$$\Delta V = I_{L\_peak} \cdot \sqrt{\frac{L_S}{C_D}} \ , \quad (3.2)$$

in which,
I_{L_peak} = peak inductor current (at maximum input voltage)
L_S = leakage inductance
C_D = total drain capacitance

Without a peak clamp ΔV depends on the leakage inductance, the total capacitance on the drain node (C_R and parasitic capacitance's C_{OSS}, C_W) and the primary peak current just before switch-off. These parameters are not known yet but assuming the ΔV would be 125V and substituting V_{IN_MAX} = 264√2V, V_{OUT} = 185V and V_F = 0.7V gives a maximum turns ratio of:

$$n \le \frac{V_{DS\_MAX} - V_{IN\_MAX} - \Delta V}{(V_{OUT} + V_F)} = \frac{800 - 264 \cdot \sqrt{2} - 125}{185.7} \le 1.62 \ . \quad (3.3)$$

Choosing the maximum turns ratio close to this value of 1.62 will give minimum switch-on losses at high input voltages. But keep in mind that the value of the ΔV should be checked afterward because this depends on the transformer construction (leakage inductance).

Step 2 calculating primary inductance L_P and resonance capacitor C_D

To simplify the formulas the commutation time is neglected and the resonance time is assumed to be constant, which is not the case when $V_{IN} < n \cdot V_{OUT}$. Now L_P and C_D can be calculated by the following formulas

$$L_P = \frac{\left(\frac{1}{f_{MIN}} - \frac{1}{f_{MAX}}\right)^2}{\left[\sqrt{2 \cdot \frac{P_{OUT\_MAX}}{h} \cdot \frac{1}{f_{MIN}}} \cdot \left(\frac{1}{V_{IN\_MIN}} + \frac{1}{n \cdot V_{OUT}}\right) - \sqrt{2 \cdot \frac{P_{OUT\_MIN}}{h} \cdot \frac{1}{f_{MAX}}} \cdot \left(\frac{1}{V_{IN\_MAX}} + \frac{1}{n \cdot V_{OUT}}\right)\right]^2} , \quad (3.4)$$

$$C_D = t_{RES}{}^2 \cdot \frac{1}{p^2 \cdot L_P} , \quad (3.5)$$

in which

$$t_{RES} = \frac{1}{f_{MIN}} - L_P \cdot \sqrt{\frac{2 \cdot P_{OUT\_MAX}}{h \cdot L_P \cdot f_{MIN}}} \cdot \left(\frac{1}{V_{IN\_MIN}} + \frac{1}{n \cdot V_{OUT}} \right). \quad (3.6)$$

Substituting two different points P_1 and P_2 in the above formulas:
P_1: f_{MIN} = 25kHz @V_{IN_MIN} = 100V_{DC}, P_{OUT_MAX} = 85W
P_2: f_{MAX} = 150kHz @V_{IN_MAX} = 373V_{DC}, P_{OUT_MIN} = 20W
This gives an L_P = 1mH and C_D = 1.17nF. In practice the capacitor also consist out of a parasitic part (e.g. C_{OSS} and C_W). Because of this an actual capacitor value of 1nF is used.

Note:
Keep in mind that the main reason for placing the resonant capacitor is to limit the **switch-off losses** and to reduce the dV/dt for EMI reasons. When using the formulas above and choosing a small frequency range (f_{MIN}…f_{MAX}) it may end up in a large capacitor value, which will result in higher **switch-on** losses (at high input voltage). In this case it is recommended to make another choice for the frequency range or the value of P_{MIN}.

step 3 defining secondary voltage/turn

The following output voltages are required: 185Vmain output, 80V, 16V and ±10V. Because the leakage inductance increases with the number of layers it is recommended to select the voltage per turn as large as possible to reduce the number of turns. Assuming N_S = 34 secondary turns for the main output gives 5.46V per turn (185.7V divided by 34 turns). In this case the other outputs requires respectively fifteen turns for the 80Voutput, three turns for the 16V output, V_{CC} winding and two turns for the 10V output.

step 4 defining primary number of turns N_P

The primary number of turns N_P is equal to:

$$N_P = n \cdot N_S$$
$$N_P = 1.62 \cdot 34 \approx 55. \quad (3.7)$$

Sense resistor

The sense resistor in series with the MOSFET limits the maximum inductor peak current. The inductor peak current is calculated by:

$$I_{L\_peak} = 2 \cdot \frac{P_{OUT}}{h} \cdot \frac{n \cdot V_{OUT} + V_{IN}}{n \cdot V_{OUT} \cdot V_{IN} \cdot \left(1 - p \cdot \sqrt{L_P \cdot C_D} \cdot f\right)}. \quad (3.8)$$

Limiting the output power to 90W and substituting $\eta = 0.9$, $n \cdot V_{OUT} = 300.5V$, $V_{IN} = 100V$, $L_P = 1mH$, $C_D = 1.17nF$ and $f = 23.8kHz$ gives an primary peak current of 2.9A

Now the sense resistor can be calculated by

$$R_{SENSE} = \frac{V_{OCP}}{I_{L\_peak}}, \quad (3.9)$$

in which V_{OCP} = the Over Current Protection level (fixed at 0.5V @ $I_{(opp)(demag)}$ >-24μA).

Substituting $V_{OCP} = 0.5V$ and $I_{L\_peak} = 2.9A$ gives a sense resistor of 172mΩ (two resistors of 330mΩ in parallel gives a maximum primary peak current $I_{L\_peak} = 3.03A$ @ $V_{IN} = 100V$). It is recommended to use low inductive current sense resistors preventing noise at the Sense pin.

Step 5 Selecting the core size

The peak flux density in the transformer can be calculated by the following equation:

$$B_{peak} = \frac{L_P \cdot I_{L\_peak}}{N_P \cdot A_{MIN}}, \quad (3.10)$$

in which
L_P = primary inductance
I_{L_peak} = primary peak current set by the OCP level
N_p = primary number of turns
A_{MIN} = minimum core area

The saturation flux density of a ferrite core (Philips 3C85) is equal to 330mT at 100°C. Substituting the previous calculated L_P, I_{L_peak} and N_P will give the minimum required core area.

$$A_{MIN} \geq \frac{L_P \cdot I_{L\_peak}}{B_{sat} \cdot N_P} \geq \frac{1 \cdot 10^{-3} \cdot 3.03}{330 \cdot 10^{-3} \cdot 55} \geq 167 mm^2 \quad (3.11)$$

E42/21/15 core can meet this requirement. The core parameters of the E42 are listed in the Table 3.1.

Table 3.1

SYMBOL	PARAMETER	VALUE	UNIT
Ve	effective volume	17300	mm^3
Ae	effective area	178	mm^2
A_{min}	minimum area	175	mm^2

The core area is mainly defined by the minimum switching frequency f_{MIN} that is chosen before.

When the core size should be reduced it is recommended to increase the minimum switching frequency and calculate the new values for L_P and C_D.

Recommendation for the transformer construction

The maximum drain source voltage is proportional to the leakage inductance L_S, which is modeled as an inductance in series with the primary inductance. This will cause an additional voltage spike across the MOSFET. Because of this it is necessary to minimize the leakage inductance. A layer transformer is a good choice regarding a low leakage inductance. Using a sandwich construction, where the primary winding is split into two windings with the secondary positioned between those two, will reduce the leakage inductance even more.

Another recommendation with respect to the transformer construction is to put the primary winding, which is connected to the drain of the MOSFET, at the inner side. In this case the other windings work as a shielding for E-field generated by this winding.

3.2 PROTECTIONS

OVP and OPP are set by currents flowing in and out of the demag pin respectively.
Each current is determined by a resistor between the Vcc winding and the Demag pin. It is possible that the correct current ratio is met with one resistor value. But if different values have to be applied than it is best to use the configuration as given in the circuit diagram. The diode makes a path for the lowest resistor value and the diode current direction determines to which protection. Anode to the Vcc winding if OVP needs the lowest value resistor.

The OVP resistor;

$$R_{OVP} = \frac{\left(\frac{N_{Vcc}}{N_S} \cdot OVP\right) - V_{clamp,demag(positive)}\langle -Vf \rangle}{I_{(ovp)(demag)}}. \qquad (3.12)$$

$\langle -Vf \rangle$ is extra addition in case a series diode has to be applied with the OVP resistor. That if the OPP resistor value is higher.

Substituting an OVP level of 1.15 x 185Vout gives a resistor value without or with a diode;

$$R_{OVP} = \frac{\left(\frac{3}{34} \cdot 1.15 \cdot 185\right) - 0.7\langle -0.6 \rangle}{60m} \approx 300k\Omega\langle 290k\Omega \rangle \qquad (3.13)$$

The OPP resistor;

OPP correction activates if the Dem current is < -24uA. See fig. 2.4.

This current is proportional with the dc line input voltage. At the lowest mains input the OPP correction should not contribute. Then the limit OCP level of 0.5V restricts the maximum output power.

$$R_{OPP} = \frac{\left(\frac{N_{Vcc}}{N_P} \cdot V_{IN(\min)}\right) + V_{clamp,demag(negative)}\langle -V_F \rangle}{24mA}.$$

(3.14)

Substituting a minimum dc input voltage threshold of 135V and, diode depending, a V_F of 0.6V will give the following resistor value:

$$R_{OPP} = \frac{\left(\frac{3}{55} \cdot 135\right) - 0.25\langle -0.6 \rangle}{24m} \approx 296k\Omega\langle 270k\Omega \rangle.$$

(3.15)

The values of Rovp and Ropp are near equal and therefore for both protections one resistor setting is used. A diode is not needed in this case.

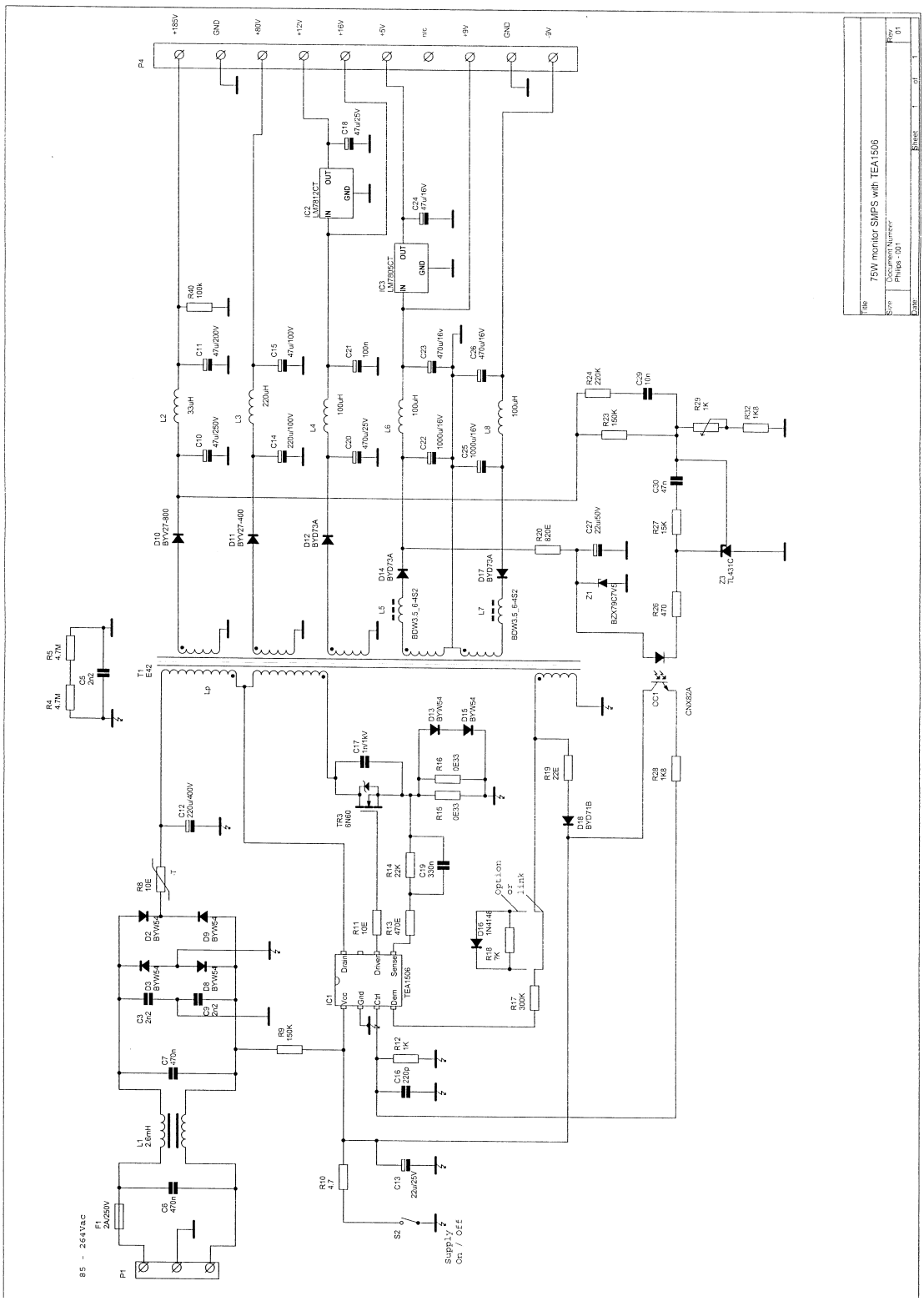
Thus Rdem = Rovp = Ropp = 300 kΩ.

In the circuit diagram the optional configuration is shown when different resistors have to be used . Based on the given diode direction the OVP is set by R17 and D16.
The OPP is set by R17 plus R18.

APPENDIX 1 SPECIFICATION

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input requirements						
V_{LINE}	line voltage	Nominal operation	85		264	V_{AC}
f_{LINE}	line frequency	Nominal operation	50		60	Hz
$P_{Standby\ mode}$	Standby power consumption	VCO mode, 5V@ 20mA and other outputs at no load			2.2	W
Output requirements						
185V	Deflection output line regulation load regulation line freq. ripple switching freq. ripple overshoot/undershoot output current	All conditions $85V_{AC}$-$264V_{AC}$ I_{out}=60mA – 300mA $85V_{AC}$, 405mA $85V_{AC}$, 405mA I_{out}=54mA–405mA visa versa		185 300	 100 100 200 20 ±1	V_{DC} mV_{DC} mV_{DC} mV_{pp} mV_{pp} V_p mA
80V	Video output output current			 100		V_{DC} mA
16V	Base-drive output output current			16 20		V_{DC} mA
12V	12V output(linear regulator) output current			12 400		V_{DC} mA
±10V	vertical deflection output, cathode heater output current			±10 0.9		V_{DC} A
5V	micro controller(linear regulator) output current			5 20		V_{DC} mA
Miscellaneous						
η	efficiency	V_{LINE} = 110Vac and 230Vac, P_{OUT} = 75W		90		%

APPENDIX 2 SCHEMATIC



APPENDIX 3 PARTS LIST

REFERENCE	VALUE	TYPE	PACKAGE	12NC
Capacitors				
C3	2.2nF	MKP3366 (Y2)	C_B6_L12.5_P10mm	2222-336-60222
C5	2.2nF	MKP3366 (Y2)	C_B6_L12.5_P10mm	2222-336-60222
C6	470nF	MKP336 (X2)	C_B15_L31_P27mm5	2222-336-10474
C7	470nF	MKP336 (X2)	C_B15_L31_P27mm5	2222-336-10474
C9	2.2nF	MKP3366 (Y2)	C_B6_L12.5_P10mm	2222-336-60222
C10	47uF	KO151	CASE_R18	2222-151-62479
C11	47uF	KO151	CASE_R18	2222-151-62479
C12	220uF	057 PSM-SI	CASE_3050	2222-057-36221
C13	22uF	037 RSM	CASE_R55_CA	2222-134-50229
C14	47uF	037 RSM	CASE_R16	2222-037-69479
C15	47uF	037 RSM	CASE_R16	2222-037-69479
C16	22nF	MKT 370	C370_A	2222-370-21223
C17	1nF	KP/MMKP376	C_B6_L18.5_P15mm	2222-375-44102
C18	47uF	097 RLP	CASE_R11_m	2222-037-56479
C19	330nF	MKT 370	C370_B	2222-370-11334
C20	470uF	136 RVI	CASE_R16	2222-136-66471
C21	100nF	MKT 370	C370_A	2222-370-11104
C22	1000uF	037 RSM	CASE_R16	2222-037-65102
C23	470uF	037 RSM	CASE_R14	2222-037-65471
C24	47uF	037 RSM	CASE_R74_m	2222-097-56479
C25	1000uF	037 RSM	CASE_R16	2222-037-65102
C26	470uF	037 RSM	CASE_R14	2222-037-65471
C27	22uF	037 RSM	CASE_R11_m	2222-037-90056
C29	10nF	MKT 370	C_B2.5_L7.2_P5mm08	2222-370-41103
C30	47nF	MKT 370	C370_A	2222-370-21473
Diodes				
D2	BYW54	control. avalanche	SOD57	9333-636-10153
D3	BYW54	control. avalanche	SOD57	9333-636-10153
D8	BYW54	control. avalanche	SOD57	9333-636-10153
D9	BYW54	control. avalanche	SOD57	9333-636-10153
D10	BYV27-600	control. avalanche	SOD57	9340-418-70113
D11	BYV27-400	control. avalanche	SOD57	9340-366-90133
D12	BYD73A	control. avalanche	SOD81	9337-537-40163
D13	BYW54	control. avalanche	SOD57	9333-636-10153
D14	BYD73A	control. avalanche	SOD81	9337-537-40163
D15	BYW54	control. avalanche	SOD57	9333-636-10153
D16 (not applied)	1N4148	general purpose	SOD27	9330-839-90153
D17	BYD73A	control. avalanche	SOD81	9337-537-40163
D18	1N4148	general purpose	SOD27	9330-839-90153
Z1	BZX79C	zener	SOD27	9331-177-60153
Z3	TL431C	voltage regulator	TO226AA	TL431C
IC's				
IC1	TEA1507	PWM controller	SOT97_s	DIL8
IC2	LM7812CT	linear stabilizer	TO220_vc	PN-LM7812CT
IC3	LM7805CT	linear stabilizer	TO220_vc	PN-LM7805CT
OC1	CNX82A	Opto-coupler	SOT231	9338-846-80127
Magnetics				
L1	2.6mH CU20d3_4	common mode choke	CU20d3	3112-338-32441
L2	33uH	Choke	TSL0707_2e	TSL0709-33K1R9
L3	220uH	Choke	uChoke_3e	LAL03NA221K
L4	100uH	Choke	TSL0707_5mm0	TSL0709-101KR66
L5	BDW3.5_6-4S2	ferrite bead		4330-030-38741
L6	100uH	Choke	TSL0707_5mm0	TSL0709-101KR66
L7	BDW3.5_6-4S2	ferrite bead		4330-030-38741
L8	100uH	Choke	TSL0707_5mm0	TSL0709-101KR66
T1	1000uH	CE422v SMPS transformer		8228-001-32811
Resistors				
R4	4.7M	VR25		2322-241-13475
R5	4.7M	VR25		2322-241-13475
R8	10	NTC		2322-594-XXXXX

R9	150k	VR25		2322-241-13154
R10	4.7	PR01		2322-193-13478
R11	10	SFR16T		2322-180-73109
R12	1k	SFR16T		2322-180-73102
R13	470	SFR16T		2322-180-73471
R14	22k	SFR16T		2322-180-73223
R15	0.33	SFR25H		RES-186-SFR25H
R16	0.33	SFR25H		RES-186-SFR25H
R17	300k	SFR16S		2322-187-53304
R18 (not applied)		SFR16S		2322-187-
R19	22	SFR16S		2322-187-53229
R20	820	SFR16T		2322-180-73821
R23	150k	SFR16T		2322-180-73154
R24	220k	SFR16T		2322-180-73224
R26	470	SFR16T		2322-180-73471
R27	15k	SFR16T		2322-180-73153
R28	1.8k	SFR16T		2322-187-73182
R29	1k	SFR16T		2322-180-73821
R32	1.8k	SFR16T		2322-180-73182
R40	100k	SFR16T		2322-180-73104
Miscellaneous				
F1	2A	fuse	GLAS_HOLDER	2412-086-28196
P1	MKS3730_2p_220V	connector (mains)		MKS3733-1-0-303
P4	MKS3730_10p	connector (output)		MKS3740-1-0-1010
S2		SPDT		FARNELL-150-559
Transistors				
TR3	STP7NB80FP	MOSFET	TO220	STP7NB80FP